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IN THE CLAIMS

Please amend claim 23 as follows below.

The following listing of claims replaces all prior versions, and listings, of claims:

1. (Previously Presented) An integrated circuit comprising:
one or more functional blocks to perform one or more functions; and
a frequency compensation circuit including
a selectively enabled reliability oscillator to generate a reference oscillating signal,
a degraded reliability oscillator to generate a degraded oscillating signal, and
a compare circuit coupled to the reliability oscillators, the compare circuit to
compare the oscillating signals and to generate a frequency compensation signal in
response to the comparison being greater than a predetermined threshold.
2. (Previously Presented) The integrated circuit of claim 1, wherein the frequency
compensation circuit further includes
a first counter coupled between the selectively enabled reliability oscillator and the
compare circuit, the first counter to generate a first reference count;
a second counter coupled between the degraded reliability oscillator and the compare
circuit, the second counter to generate a second degraded count; and
the compare circuit to compare the first reference count with the second degraded count.
3. (Previously Presented) The integrated circuit of claim 2, wherein the frequency
compensation circuit further includes
a first prescaler coupled between the selectively enabled reliability oscillator and the first
counter, the first prescaler to divide by N the number of oscillations in an oscillating signal from
the selectively enabled reliability oscillator; and
a second prescaler coupled between the dynamic reliability oscillator and the second
counter, the second prescaler to divide by N the number of oscillations in an oscillating signal
from the degraded reliability oscillator.

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4. (Previously Presented) The integrated circuit of claim 1, wherein
the degraded reliability oscillator is a clocked reliability oscillator to generate an AC degraded oscillating signal; and
the frequency compensation circuit further includes a static reliability oscillator to generate a DC bias degraded oscillating signal.
5. (Previously Presented) The integrated circuit of claim 4, wherein the frequency compensation circuit further includes
a first counter coupled between the selectively enabled reliability oscillator and the compare circuit, the first counter to generate a reference count;
a second counter coupled between the clocked reliability oscillator and the compare circuit, the second counter to generate a dynamic count;
a third counter coupled between the static reliability oscillator and the compare circuit, the third counter to generate a static count; and
the compare circuit to compare the reference count with the dynamic count and the reference count with the static count.
6. (Previously Presented) The integrated circuit of claim 5, wherein the frequency compensation circuit further includes
a first prescaler coupled between the selectively enabled reliability oscillator and the first counter, the first prescaler to divide by N the number of oscillations in an oscillating signal from the selectively enabled reliability oscillator;
a second prescaler coupled between the dynamic reliability oscillator and the second counter, the second prescaler to divide by N the number of oscillations in an oscillating signal from the dynamic reliability oscillator; and
a third prescaler coupled between the static reliability oscillator and the third counter, the third prescaler to divide by N the number of oscillations in an oscillating signal from the static reliability oscillator.

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7. (Original) The integrated circuit of claim 1, wherein the integrated circuit is a microprocessor.
8. (Previously Presented) The integrated circuit of claim 1, wherein
the degraded reliability oscillator is a static reliability oscillator to generate a DC bias degraded oscillating signal, and
the compare circuit to compare the reference oscillating signal and the DC bias degraded oscillating signal to generate the frequency compensation signal in response to the comparison being greater than the predetermined threshold.
9. (Previously Presented) The integrated circuit of claim 8, wherein the frequency compensation circuit further includes
a first counter coupled between the selectively enabled reliability oscillator and the compare circuit, the first counter to generate a reference count;
a second counter coupled between the static reliability oscillator and the compare circuit, the second counter to generate a static count; and
the compare circuit to further compare the reference count with the static count.
10. (Previously Presented) The integrated circuit of claim 9, wherein the frequency compensation circuit further includes
a first prescaler coupled between the selectively enabled reliability oscillator and the first counter, the first prescaler to divide by N the number of oscillations in an oscillating signal from the selectively enabled reliability oscillator; and
a second prescaler coupled between the dynamic reliability oscillator and the second counter, the second prescaler to divide by N the number of oscillations in an oscillating signal from the static reliability oscillator.
11. (Original) The integrated circuit of claim 8, wherein the integrated circuit is a microprocessor.

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12. (Previously Presented) An integrated circuit comprising:
one or more functional blocks to perform one or more functions; and
a frequency compensation circuit including
a first reliability oscillator including a selectively powered on ring oscillator to
avoid transistor degradation, the first reliability oscillator to generate a reference
oscillating signal on a first oscillation output,
a second reliability oscillator including a powered ring oscillator to experience
transistor degradation, the second reliability oscillator to generate a degraded oscillating
signal on a second oscillation output, and
a compare circuit to compare the reference oscillating signal and the degraded
oscillating signal to generate a frequency compensation signal in response to the
comparison being greater than a predetermined threshold.
13. (Previously Presented) The integrated circuit of claim 40, wherein the frequency
compensation circuit further includes
a first prescaler coupled between the first reliability oscillator and the first counter, the
first prescaler to divide by N the number of oscillations in the reference oscillating signal; and
a second prescaler coupled between the second reliability oscillator and the second
counter, the second prescaler to divide by N the number of oscillations in the degraded
oscillating signal.
14. (Previously Presented) The integrated circuit of claim 40, wherein the second reliability
oscillator includes
a powered static ring oscillator to experience DC static transistor degradation,
the degraded oscillating signal is a DC bias degraded oscillating signal on the second
oscillation output, and
the degraded count is a static count.
15. (Previously Presented) The integrated circuit of claim 40, wherein

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the second reliability oscillator includes a powered clocked ring oscillator to experience AC dynamic transistor degradation,

the degraded oscillating signal is an AC degraded oscillating signal on the second oscillation output, and

the degraded count is a dynamic count.

16. (Previously Presented) The integrated circuit of claim 15, wherein the frequency compensation circuit further includes

a third reliability oscillator including a powered static ring oscillator to experience DC static transistor degradation, the third reliability oscillator to generate a DC bias degraded oscillating signal on a third oscillation output, and

a third counter having an input to couple to the third oscillation output, the third counter to generate a static count on a third count output.

17. (Previously Presented) The integrated circuit of claim 16, wherein the frequency compensation circuit further includes

a first prescaler coupled between the first reliability oscillator and the first counter, the first prescaler to divide by N the number of oscillations in the reference oscillating signal,

a second prescaler coupled between the second reliability oscillator and the second counter, the second prescaler to divide by N the number of oscillations in the dynamic oscillating signal, and

a third prescaler coupled between the third reliability oscillator and the third counter, the third prescaler to divide by N the number of oscillations in the static oscillating signal.

18. (Previously Presented) The integrated circuit of claim 13, wherein the frequency compensation circuit further includes a state machine to start and stop the counting by the counters.

19. (Previously Presented) The integrated circuit of claim 13, wherein

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the first counter includes a count overflow output and a count enable input, the count overflow output being a stop signal is coupled to the count enable input to stop the first counter from counting further, and

the frequency compensation circuit further includes a first synchronizer having an input coupled to the count overflow output and an output coupled to a count enable input of the second counter, the first synchronizer to synchronize the stop signal to stop the second counter from counting further.

20. (Previously Presented) The integrated circuit of claim 16, wherein

the first counter includes a count overflow output and a count enable input, the count overflow output being a stop signal is coupled to the count enable input to stop the first counter from counting further, and

the frequency compensation circuit further includes

a first synchronizer having an input coupled to the count overflow output and an output coupled to a count enable input of the second counter, the first synchronizer to synchronize the stop signal to stop the second counter from counting further, and

a second synchronizer having an input coupled to the count overflow output and an output coupled to a count enable input of the third counter, the second synchronizer to synchronize the stop signal to stop the third counter from counting further.

21. (Original) The integrated circuit of claim 12, wherein a clock signal is coupled into a clock input of the second reliability oscillator.

22. (Original) The integrated circuit of claim 12, wherein the integrated circuit is a microprocessor.

23. (Currently Amended) A method in an integrated circuit with functional blocks, the method comprising:

enabling measurement of frequencies of two reliability oscillators;

measuring a first frequency of a first reliability oscillator having non-stressed transistors;

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measuring a second frequency of a second reliability oscillator having stressed transistors;
and
comparing the first frequency with the second frequency to determine a first measure of transistor degradation.

24. (Previously Presented) The method of claim 23, wherein the stressed transistors of the second reliability oscillator are dynamically stressed transistors.

25. (Previously Presented) The method of claim 23, wherein the stressed transistors of the second reliability oscillator are statically stressed transistors.

26. (Previously Presented) The method of claim 25, further comprising
enabling measurement of a frequency of a third reliability oscillator;
measuring a third frequency of the third reliability oscillator having dynamically stressed transistors; and
comparing the first frequency with the third frequency to determine a second measure of transistor degradation.

27. (Original) The method of claim 23 further comprising: performing one or more functions with the functional blocks.

28. (Original) The method of claim 27, wherein
the functional blocks include an execution unit to execute instructions; and
the integrated circuit is a microprocessor.

29. (Previously Presented) The method of claim 23, wherein the first reliability oscillator and the second reliability oscillator have substantially similar circuits.

30. (Previously Presented) The method of claim 29, wherein
the second reliability oscillator has degraded transistors; and

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the first reliability oscillator has transistors without degradation.

31. (Original) The method of claim 23, wherein
the comparing determines a new clock ratio, and
if the new clock ratio is less than an initial clock ratio multiplied by a guard band, then
the new clock ratio is output to a clock generator.
32. (Original) The method of claim 31, further comprising generating a clock signal using
the new clock ratio.
33. (Previously Presented) A microprocessor integrated circuit comprising:
one or more functional blocks to perform one or more functions; and
a frequency compensation circuit including
a reference reliability oscillator to selectively generate a reference oscillating
signal,
a degrading reliability oscillator to selectively generate a degraded oscillating
signal, and
a measurement and comparison circuit coupled to the reliability oscillators, the
measurement and comparison circuit to receive the reference oscillating signal and the
degrading oscillating signal to generate a first measure of transistor degradation.
34. (Original) The microprocessor integrated circuit of claim 33, wherein the degrading
reliability oscillator is a dynamic reliability oscillator that selectively generates an AC degraded
oscillating signal.
35. (Original) The microprocessor integrated circuit of claim 33, wherein the degrading
reliability oscillator is a static reliability oscillator that selectively generates a DC degraded
oscillating signal.

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36. (Previously Presented) The microprocessor integrated circuit of claim 35, wherein the frequency compensation circuit further includes
- a dynamic reliability oscillator to selectively generate an AC degraded oscillating signal,
 - and
 - the measurement and comparison circuit further to receive the reference oscillating signal and the AC degraded oscillating signal to generate a second measure of transistor degradation.
37. (Original) The microprocessor integrated circuit of claim 36, wherein the measurement and compare circuit further to compare the first measure of transistor degradation with the second measure of transistor degradation to determine a worst transistor degradation.
38. (Original) The microprocessor integrated circuit of claim 37, wherein the measurement and compare circuit to generate a frequency compensation signal in response to the worst transistor degradation being greater than a predetermined level.
39. (Previously Presented) The integrated circuit of claim 1, wherein
- the degraded reliability oscillator is a clocked reliability oscillator to generate an AC degraded oscillating signal; and
 - the compare circuit to compare the reference oscillating signal and the AC degraded oscillating signal to generate the frequency compensation signal in response to the comparison being greater than the predetermined threshold.
40. (Previously Presented) The integrated circuit of claim 12, wherein
- the frequency compensation circuit further includes
 - a first counter having an input to couple to the first oscillation output, the first counter to generate a reference count on a first count output, and
 - a second counter having an input to couple to the second oscillation output, the second counter to generate a degraded count on a second count output; and
 - the compare circuit to compare the reference count and the degraded count to compare the reference oscillating signal and the degraded oscillating signal to generate the frequency

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compensation signal in response to the comparison of the counts being greater than a predetermined threshold.

41. (Previously Presented) The integrated circuit of claim 1, wherein each of the reliability oscillators includes a ring oscillator.

42. (Previously Presented) The microprocessor integrated circuit of claim 33, wherein each of the reliability oscillators includes a ring oscillator.

43. (Previously Presented) The microprocessor integrated circuit of claim 33, wherein the one or more functional blocks includes an execution unit to execute instructions.

44. (Previously Presented) The integrated circuit of claim 12, wherein the powered ring oscillator of the second reliability oscillator is powered on with the integrated circuit.

45. (Previously Presented) The integrated circuit of claim 14, wherein the powered static ring oscillator of the second reliability oscillator is powered on with the integrated circuit.

46. (Previously Presented) The integrated circuit of claim 15, wherein the powered clocked ring oscillator of the second reliability oscillator is powered on with the integrated circuit.

47. (Previously Presented) The integrated circuit of claim 16, wherein
the powered clocked ring oscillator of the second reliability oscillator is powered on with the integrated circuit, and
the powered static ring oscillator of the third reliability oscillator is powered on with the integrated circuit.

48. (Previously Presented) The method of claim 23, wherein
the first reliability oscillator includes a first ring oscillator and the first frequency is a first ring oscillator frequency, and

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the second reliability oscillator includes a second ring oscillator and the second frequency is a second ring oscillator frequency.

49. (Previously Presented) The method of claim 26, wherein

the first reliability oscillator includes a first ring oscillator and the first frequency is a first ring oscillator frequency,

the second reliability oscillator includes a second ring oscillator and the second frequency is a second ring oscillator frequency, and

the third reliability oscillator includes a third ring oscillator and the third frequency is a third ring oscillator frequency.